

e20-040 braindumps

EMC Technology Foundations

e20-040: emc technology foundations

Practice Exam: e20-040 Exams

Exam Number/Code: e20-040

Exam Name: emc technology foundations

Questions and Answers: 237 Q&As

([Technology Foundations](#))



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Exam : EMC E20-040

Title : EMC (r) Technology Foundations

1. Which type of protection is only used for mainframes?

- A.RAID 1
- B.RAID 5
- C.RAID 10
- D.Parity RAID

Answer: C

2. After a split operation has occurred, where is the information maintained for changes to the standard volume and BCV?

- A.PSM LUN
- B.track tables
- C.vault
- D.VDEV tables

Answer: B

3. In a NetWorker environment, which EMC Disk Library feature is used to export virtual tapes to physical tapes, while preventing blind spots?

- A.Auto Archive
- B.Embedded Storage Node
- C.Embedded Media Server
- D.Remote Copy

Answer: B

4. In a CLARiiON array, what is a characteristic of a metaLUN?

- A.Can be only expanded one time
- B.Can be used with SnapView and MirrorView
- C.Cannot be added to a storage group
- D.Supported on FC and CX series arrays

Answer: B

5. After Rainfinity completes a directory or share move, clients can access data through a logical view without having to remap to the new destination. What is the underlying physical location called that maps this logical view?

- A.Data Mobility
- B.Global Namespace
- C.Proxy Service
- D.VLAN Change

Answer: B

6. What is a characteristic of a Content Address in Centera?

- A. Administrator generated
- B. File system based
- C. Inherently stable
- D. Location-dependent

Answer: C

7. Which Symmetrix implements a unified director feature?

- A. DMX1000
- B. DMX2000
- C. DMX-3
- D. Symmetrix 8000

Answer: C

8. What is a DMX-3 Direct Matrix Interconnect specification?

- A. 64 2 Gb/s Fibre Channel paths
- B. 128 direct paths from directors and memory
- C. Four or eight processors per director
- D. Full component-level redundancy with hot-swappable replacements

Answer: B

9. Which SAN topology requires a direct link from any switch to every other switch in the fabric?

- A. Compound core-edge
- B. Full mesh
- C. Partial mesh
- D. Simple core-edge

Answer: B

10. How are DMX-2 global cache director boards divided?

- A. Boards are divided into four addressable memory chips
- B. Boards are divided into four addressable regions comprised of one memory chip
- C. Boards consist of four memory chips, each divided into eight regions
- D. Boards consist of memory chips and are divided into four addressable regions

Answer: D

11. In a CLARiiON array, how is I/O handled when a LUN is expanding?

- A. Continues to all component LUNs
- B. Continues to base LUN only
- C. Halted during expansion
- D. Halted to the base LUN only

Answer: B

12. When changes are made to a SnapView source LUN, where is the original data saved?

- A. Cache memory
- B. Clone Private LUN
- C. PSM
- D. Reserved LUN pool

Answer: D

13. Which are the characteristics of Symmetrix Engenuity?

- A. Comprehensive Symmetrix management and data security
- B. Continuous availability, data integrity, built-in security features

- C.Enabled consistency and continuous availability
- D.Symmetrix-based feature portability and enabled consistency

Answer: B

14. Which DMX is optimized for the most efficient power and cooling?

- A.DMX-2
- B.DMX-3 950
- C.DMX3000
- D.DMX800

Answer: B

15. PowerPath is connected to Storage Processor A and Storage Processor B. What action does PowerPath take when one path to Storage Processor A fails?

- A.Redirects the I/O load across the remaining three paths to the array
- B.Redirects the I/O through the two paths to Storage Processor B
- C.Trespasses the LUN to Storage Processor B and uses the two paths through this Storage Processor
- D.Uses the one remaining path through Storage Processor A

Answer: D

16. Which mechanism is used shorten the synchronization process after the link goes down between the primary and secondary mirrors?

- A.Fracture log
- B.Persistent Storage Manager
- C.Primary arrays write cache
- D.Reserved LUN pool

Answer: A

17. What is the cause of the delay in a DMX-3 read miss?

- A.Host missed the time to get data
- B.Information is missing from the files
- C.Information left cache before it was read
- D.Information must be read from disk

Answer: D

18. How many bi-directional mirror relationships are allowed per CLARiiON array?

- A.1
- B.2
- C.4
- D.8

Answer: C

19. In a CLARiiON array, which clone state would prevent a clone from being removed from a clone group?

- A.Consistent
- B.Fractured
- C.Promoted
- D.Synchronizing

Answer: D

20. Which operation must an NFS client perform to access a Celerra advertised connection point?

- A.Export
- B.Map
- C.Mount
- D.Share

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